DVB-S2 Demodulator VHDL RTL/structural Macro

Technical Specifications

- DVB-S2 Macro is a DVB-S2 Demodulator VHDL design capable of Demodulating, on a single FPGA device of a suitable family, in CCM, VCM and ACM modes DVB-S2 Traffic at BB Frames level for the supported MODCODs up to a Baud Rate of 50Msps.
- The Demodulator macro is highly complete since includes other than the standard DVB-S2 functional blocks also the Outdoor to Indoor Cable Slope Equalizer, IQ Gain and Phase Unbalance Equalizer, Group Delay Distortion Equalizer, SNIR estimator for ACM mode. Correlated also to this Macro is the DVB-S2 Test Modulator Macro capable of providing the DVB-S2 BBFrame formatting together with a FER Meter capable of benchmarking the acquisition and tracking performances of Macro itself. The LDPC Decoder is statistical and it is based on a parallel N=360 PNU (Processing Node Units) implementation targeted for high baud rates.
- The Macro supports the following MODCODs with the associated tested performances at the 45Mbaud (close to the maximum allowed 50Mbaud symbol rate)

MODCOD	Spectral Efficiency	DVB-S2 Standard Ideal QeF Es/No (Note[1])	Macro IL@45Mbaud Ideal AWGN (Note[2])	Macro IL@45Mbaud Non Linear Channel & Distortion(Note[3])
QPSK 1/4	0,490243	-2.350	1.25	1.15
QPSK 1/2	0,988858	1.000	0.30	0.50
QPSK 2/3	1,322253	3.100	0.10	0.40
QPSK 4/5	1,587196	4.680	0.30	0.40
8PSK 3/5	1,779991	5.500	0.90	1.40
8PSK 2/3	1,980636	6.620	0.80	1.40
8PSK 3/4	2,228124	7.910	0.40	1.10
16APSK 2/3	2,637201	8.970	0.90	1.90
16APSK 3/4	2,966728	10.210	0.70	2.10
16APSK 4/5	3,165623	11.030	0.70	2.30
16APSK 5/6	3,300184	11.610	0.70	2.40
32APSK 3/4	3,703293	12.73	0.80	2.70

Table 1

Note[1] Ideal means synchronous open loop Demodulator and Deterministic LDPC decoder AWGN channel only (i.e. no frequency error, no non linear distortion no Phase Noise, no Group Delay distortion, no Cable Losses, no I and Q phase and gain unbalance)

Note[2] Being the LDPC decoder statistical reducing the baud rate allows the average number of LDPC iteration to increase so to achieve lower IL (Implementation Losses).

Note[2] Non Lineat Channel and Distortion means : *Frequency Offset Error 5MHz, IQ Gain Unbalance 1.5dB, IQ Phase Unbalance 5 degrees, Cable Slope Distortion 2.5 dB/45MHz*

Phase Noise as DVB-S2 Mask, TWTA as DVB-S2 non linearized characteristic, Clock Error 100 ppm, Roll Off 0.35. Macro enable equalizers : IQ Equalizer, Cable Slope Equalizer, GD CMA Equalizer, Constellation Precompensation at Mapper Level in TX.

For any additional information contact:

- fax : +39-06-5587394
- phone : +39-06-5582904
- e-mail : sales@spacetechnology.it

- The PL Frame Synchronizer ROC (Receiver Operating Characteristic) at an Eb/No of -2dB for different MODCODs and for an initial frequency error equal to 20% of the Symbol Rate is reported on the left side of Fig.1. The Demodulator Acquisition Time Performances are reported instead on the right side of Fig.1 as function of the Es/No.

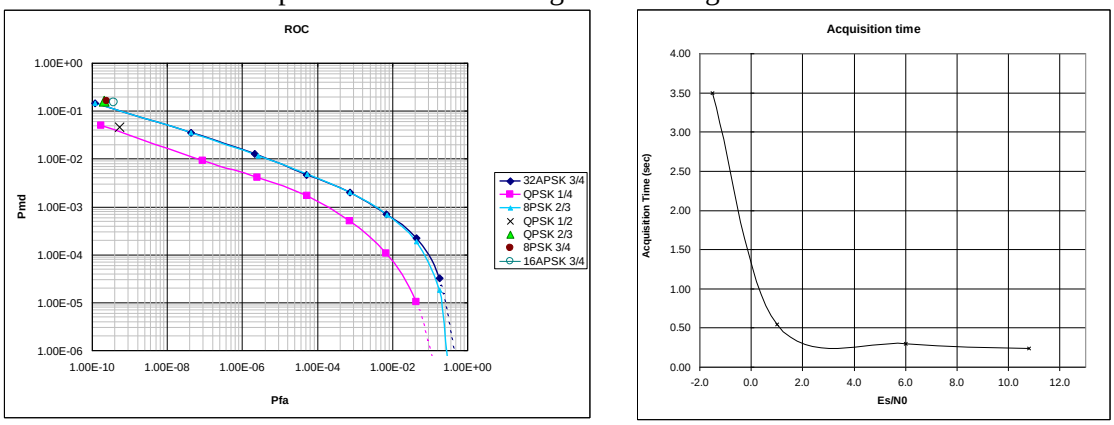

Fig. 1

- The Demodulator is also provided with a Programmable Rate adapter that allows, with a fixed digital system clock rate system, adapting the Baud Rate from 10Msps to 45Msps according to the right side curve of Fig. 2.

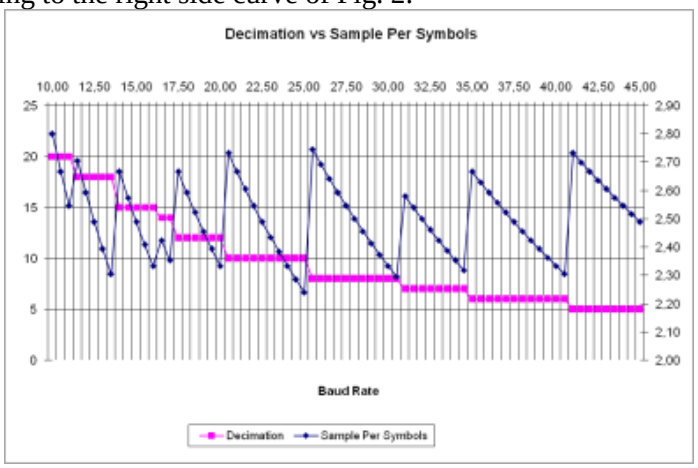

Fig. 2

- The Macro has been integrated together with the DVB-S2 Modulator and tested in several platforms and for different FPGAs, and it can be provided with an HW demonstrator based on a Software Defined Radio Board (P3U produced by Space Technology) in a 3U Form Factor (16 cm. by 10 cm. see Fig. 2 left side). The SDR demonstrator Board Data Sheet can be downloaded from Internet at http://www.spacetechnology.it/docs/Brochure%20S4MDM1.5%20rev%205.0.pdf

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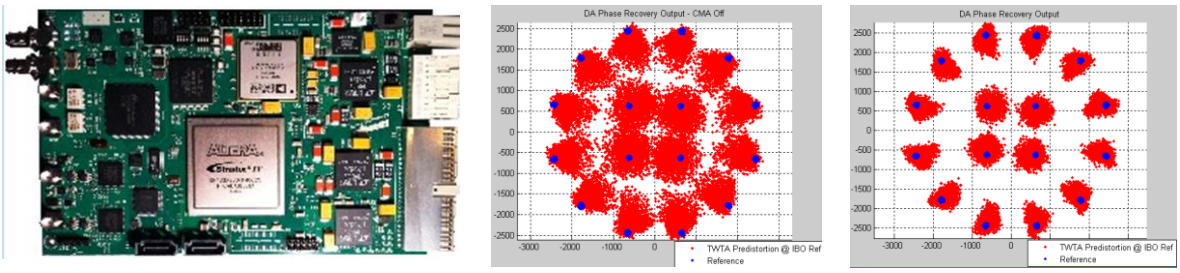

Fig. 2

- Together with the ALTERA STRATIX IV device below reported, the demonstrator target Board (SDR Board see Fig. 2) is equipped with two 12 bits DACs sampling any to rate up 0.6Gsps and two 8 bits ADCs sampling any rate up to 1.5Gsps, a Floating Point Analog Devices DSP clocked at 0.6GHz and a 512K x 36 bits Static RAM (therefore a single Modem Board).
- The macro can be provided also with a configurable Channel impairment real time VHDL modeler implementing TWTA AM-AM and AM-PM Distortion, Frequency Error, Cable Slope Distortion, Gain and Phase unbalance Distortion, DVB-S2 standard Phase Noise Mask distortion, DVB-S2 standard Group Delay distortion, so to appreciate the effect of the several Adaptive Equalizers embedded in the Macro. Right side of Fig. 2 shows the effect of CMA Equalizer (central Scattering Diagram is without the Equalizer on) with TWTA pre-compensation assuming w.r.t. the non linear distortion of the DVB-S2 standard an IBO=2.74 dB and an OBO=1.33dB for the 16APSK Modulation format.
- The macro can be provided either with complex Base Band RX and TX output for interfacing direct RF analog IQ Modulator and Demodulators or low IF @140MHz. The macro supports SRRC Filters with roll-off 0.2, 0.25, 0.3 and 0.35. The Demodulator Macro with complex Base Band ADC interface, including all the receiver Equalizer and the segment of Channel Emulator embedded on the Receiver side of the Macro (Thermal Noise Generator and Phase Noise Generator), occupies on the FPGA of the ST SDR, i.e. a STRATIX IV EP4SGX230KF40C3N device, the following Table 2 HW resources.

	Register	**Logic**	**DSP Block**	**Memory**
BB Demodulator	8.6%	8.1%	0.6%	0.3%
ACM Demodulator	17.1%	9.9%	17.0%	5,9%
Soft Demodulator	0.7%	0.7%	0.6%	31.5%
LDPC Decoder	31.2%	21.6%	0.1%	19.8%
BCH Decoder	2.3%	1.7%	0.0%	1.4%
Other	10.0%	10.0%	10.0%	10.0%
Free	30.2%	48.0%	71.7%	31.0%
Total	171.000	171.000	1.288	14.625.729

Table 2

- Although the system tests performances reported in Table 1 are taken at 45Mbaud the post layout Timing Analysis (see Table 3), for the same STRATIX IV ALTERA FPGA shows that the Macro can achieve 50Mbaud.

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Clock Domain	Target Clock Frequency for 50Mbaud	Post Layout Clock Frequency	Processing Blocks driven
clk_adc	150MHz	227Mz	Complex ADC interface BB Filtering (rate adapter and decimator of Fig. 2)
clk_dem1	125MHz	190MHz	Timing Recovery at greater than 2 samples per symbol (2.5 for 50Mbaud) other blocks see Fig. 3 below
clk_dem2	65MHz	158MHz	All the blocks at 1 sample per symbol after the Cable Slope Equalizer (Fig. 3)
clk_soft_dem	200MHz	205MHz	Soft Demodulator clock
clk_ldpc_dec	150MHz	200MHz	LDPC Decoder core clock
clk_bch_dec	200MHz	241MHz	BCH Decoder core clock
service_clk	100MHz	193MHz	Macro service clock for communication and control logic

Table 3

- Currently with an LDPC core clock of 150MHz, the Statistical LDPC Decoder guarantees 50 iterations for each of the Modulation supported by DVB-S2 standard (QPSK, 8PSK, 16APSK and 32APSK) at 50Mbauds. Nevertheless reducing the symbol rate for specific low rate applications and enlarging the LDPC statistical Decoder input buffer beyond 4.5 Frames (Table 2 shows that yet 31% of the FPGA internal memory is available) will reduce the Implementation Losses reported in Table 1. Higher than 50Mbaud rates could be achieved using an LDPC core clock of 200MHz as deemed possible according to Table 3 post layout static analysis on the ALTERA STRATIX IV or narrower CMOS geometries FPGAs.

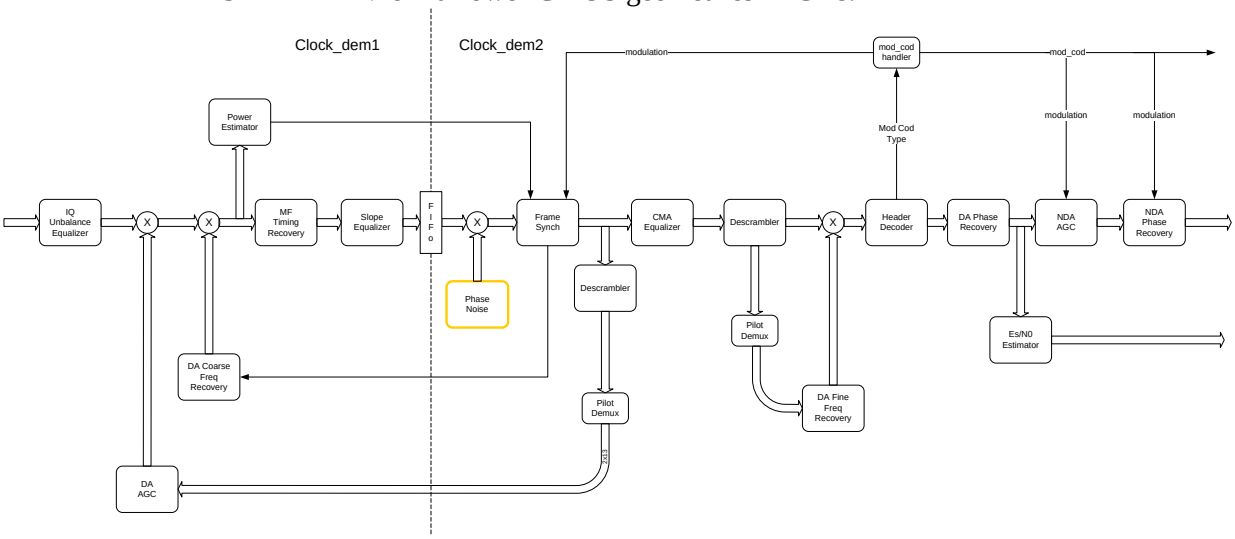

Fig. 3

- The Macro has been tested by ST customer as ACM Demodulator in a real 2 way link with Generic Stream Encapsulation Traffic Generator and a DVB-RCS return link. Assuming a given SNIR profile (caused by atmospheric fading during ACM Test) the DVB-S2 Macro controlled by the SNIR estimation returned on the DVB-RCS channel showed the frame by frame ACM switching capability reported in Fig. 4 maintaining QeF performances all test session long.

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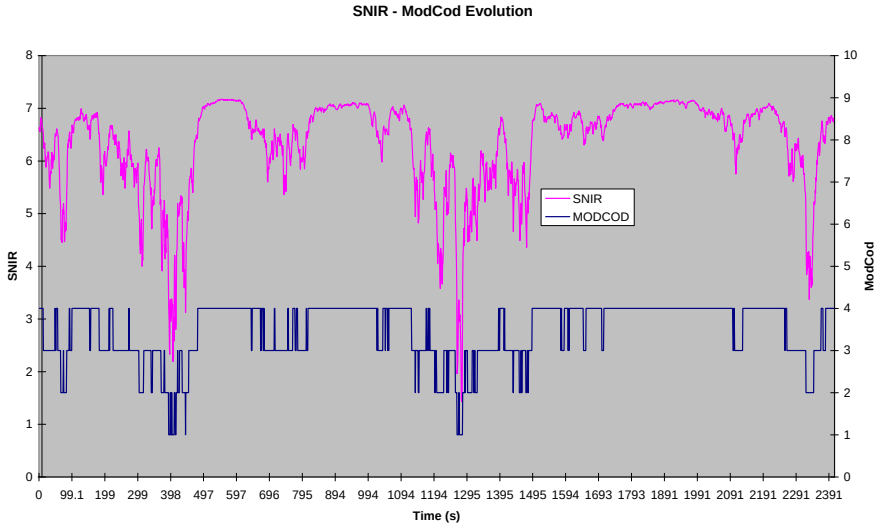

MODCOD	Code
1/4 QPSK	0
1/2 QPSK	1
2/3 QPSK	2
4/5 QPSK	3
3/5 8PSK	4
2/3 8PSK	5
3/4 8PSK	6
2/3 16APSK	7
3/4 16APSK	8
4/5 16APSK	9
5/6 16APSK	10

Fig. 4

- The DVB-S2 Demodulator Macro is available either as source VHDL RTL code, as well as structural FPGA configuration file Macro for the FPGAs that can fit its module resources.
- Finally, if needed, the Space Technology Design Team is willing to deal any feasible customization of the DVB-S2 Receiver Macro aimed at reducing the FPGA Module count and the power consumption for a lower baud rate application and smaller FPGA devices and/or to fit the Macro in different FPGA devices other than the one reported in this Macro Data Sheet.

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