DVB-S2 Modulator and Channel Emulator VHDL RTL/structural Macro

Technical Specifications

- DVB-S2 Macro is a DVB-S2 Modulator and Channel Emulator VHDL design capable of Modulating, on a single FPGA device of a suitable family, in CCM, VCM and ACM modes DVB-S2 Traffic at BB Frames level for the supported MODCODs up to a Baud Rate of 50Msps.
- The Demodulator macro is highly complete since includes other than the standard DVB-S2 functional Modulator blocks plus as additional accessory up to 27.5Mbauds the TWTA AM-AM and AM-PM distortion modeler, Transponder IMUX OMUX Group Delay and Frequency offset errors. Note that the Gain and Phase unbalance of the direct Modulator or Demodulator, if used on the RX section the Cable Slope distortion, together with Phase Noise Mask of DVB-S2 and the Thermal Gaussian Noise are provided as Channel Macro option for the Demodulator section due to their lower sample rate. Therefore those last effects could be introduced also at 50Mbaud.
- Additional Macro option of the Modulator (whose benefit in terms of performances can be evaluated only having purchased the Channel Modeler that models in real time the on Board PA distortions) is the TWTA Characteristic Inversion and Constellation Pre-distortion aimed at counteracting the strong saturation driven of the Payload TWTA
- The Modulator Macro supports the following MODCODs with the associated tested performances at the 45Mbaud (close to the maximum 50Mbaud symbol rate) reported in the DVB-S2 Demodulator Macro Data Sheet.

MODCOD	Spectral Efficiency
QPSK 1/4	0,490243
QPSK 1/2	0,988858
QPSK 2/3	1,322253
QPSK 4/5	1,587196
8PSK 3/5	1,779991
8PSK 2/3	1,980636
8PSK 3/4	2,228124
16APSK 2/3	2,637201
16APSK 3/4	2,966728
16APSK 4/5	3,165623
16APSK 5/6	3,300184
32APSK 3/4	3,703293

Table 1

- The DVB-S2 Modulator Macro architecture is reported in Fig. 1. It includes all the layers of the DVB-S2 Modulation standard, starting from plain data Traffic and generating the BBFrames up to the Base Band Modulated SRRC Filtered samples.

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- The DVB-S2 Modulator Macro can be provided either Base Band to drive at four samples per symbols (therefore max 200MHz) a couple of DACs and an RF Quadrature Modulator as reported in Fig. 1. Alternatively it can be accompanied by an IF 140MHz digital up converter sampling at 600MHz on a single real DAC. The additional Digital IF up conversion macro will take the Base Band modulator output and it will implement a Carrier NCO frequency offset (by 10MHz) then a 3/4 rate adapter FIR Filter and then finally an Fs/4 up converter. The resulting signal will be centered at IF 140MHz.

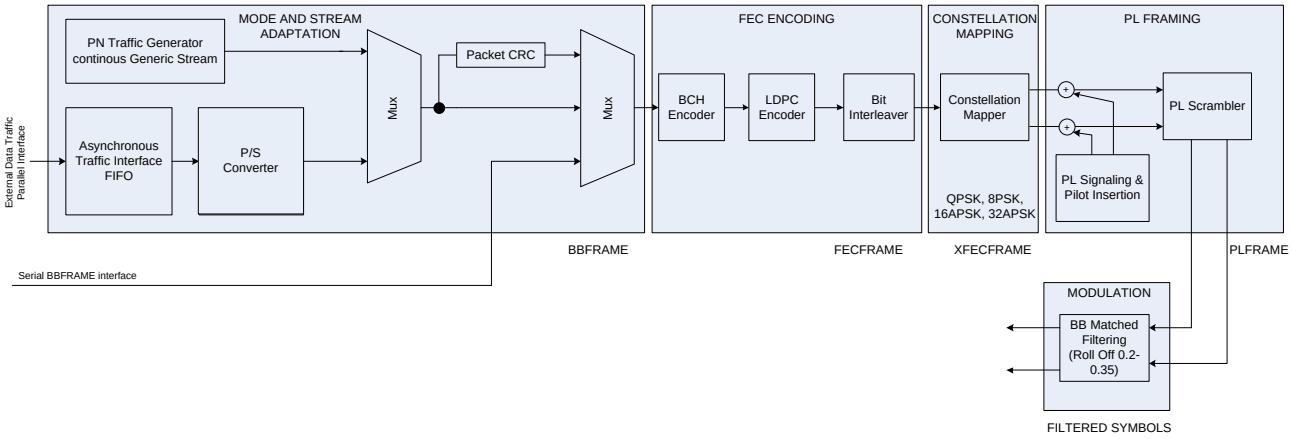

Fig. 1 DVB-S2 Modulator Macro

- The Macro has been integrated together with the DVB-S2 Demodulator and tested in platforms aimed for different FPGAs. The Macro can be provided with an HW demonstrator based on a Software Defined Radio Board (P3U produced by Space Technology) in a 3U Form Factor (16 cm. by 10 cm. see Fig. 2 left side). The SDR demonstrator Board Data Sheet can be downloaded from Internet at http://www.spacetechnology.it/docs/Brochure%20S4MDM1.5%20rev%205.0.pdf

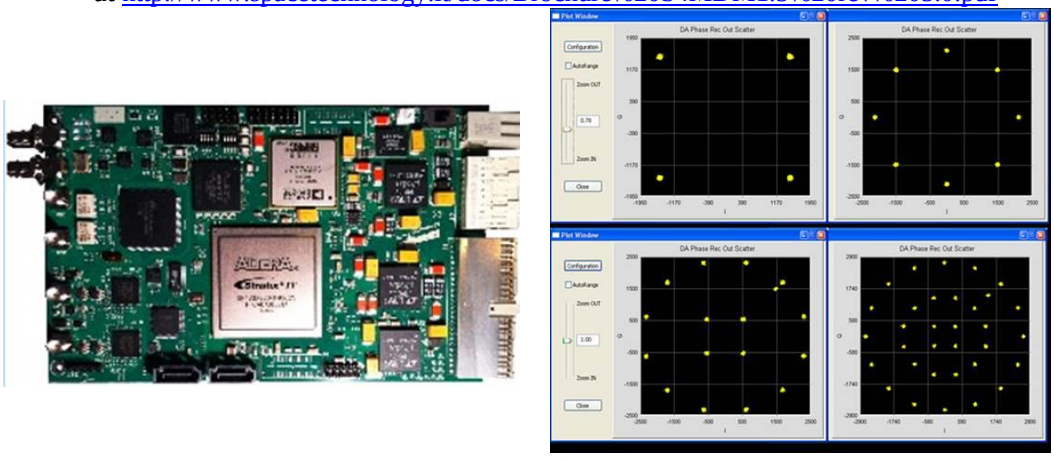

Fig. 2

- Together with the ALTERA STRATIX IV device below reported, the demonstrator target Board (SDR Board see Fig. 2) is equipped with two 12 bits DACs sampling any to rate up 0.6Gsps and two 8 bits ADCs sampling any rate up to 1.5Gsps, a

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Floating Point Analog Devices DSP clocked at 0.6GHz and a 512K x 36 bits Static RAM (therefore a single Modem Board).

- As anticipated the macro can be provided either with complex Base Band TX output for interfacing direct RF analog IQ Modulator or low IF @140MHz. The macro supports SRRC Filters with roll-off 0.2, 0.25, 0.3 and 0.35. The Modulator Macro with complex Base Band DAC interface including all block reported in the Architecture of Fig. 1 for all the four DVB-S2 supported modulations (see in Fig. 2 the Scattering Diagram of the Modulator output as demodulated by the DVB-S2 Demodulator Macro at the output of the Carrier Phase Recovery loop in absence of Thermal Noise and only with Quantization Noise) occupies on the FPGA of the ST SDR, i.e. a STRATIX IV EP4SGX230KF40C3N device, the following Table 2 HW resources.

	Register	**Logic**	**DSP Block**	**Memory**
Modulator	5.0%	4.0%	4.0%	18%
Other	1.0%	1.0%	1.0%	1.0%
Free	94.0%	95.0%	95.0%	71.0%
Total	171.000	171.000	1.288	14.625.729

Table 2

- The post layout Timing Analysis of the DVB-S2 Modulator Macro (see Table 3), for the same STRATIX IV ALTERA FPGA shows that the Macro can achieve 75Mbaud (being the Symbol Frequency interpolation section could run as post layout up to 303MHz that at 4 samples per symbol could represent 75Mbaud) although it has been tested only up to 50Mbaud corresponding to the maximum achievable baud rate of the companion DVB-S2 Demodulator Macro always provided by Space Technology.

Clock Domain	**Target Clock Frequency for 50Mbaud**	**Post Layout Clock Frequency**	**Processing Blocks driven**
clk_dac	200MHz	303Mz	Complex DAC interface BB Filtering (and four samples per complex symbol)
clk_byte	60MHz	335MHz	This clock is aimed for formatting up to FECFRAME Boarder
service_clk	100MHz	309MHz	Macro service clock for communication and control logic

Table 3

- The Channel Emulator Macro modeled on the Modulator side is instead an optional and additional processing block aimed at modeling the TWTA non-linear AM-AM and AM-PM distortion the Group Delay distortion introduced by the Satellite Transponder through the IMUX and OMUX On Board filters. Its architecture is reported in Fig. 3. As it may be easily noticed due to the presence of IMUX and OMUX IIR Filters necessary to model the Group Delay distortion a rate update from 4 samples per symbols (sampling rate of the Modulator Macro as stand-alone part) to 10 samples per symbols is necessary. This explains why the Channel Modeler is supplied up to 27.5Msps corresponding to the existing Satellites TV Transponder by

36MHz of bandwidth at roll off 0.30, of which the IMUX and OMUX filter distortion are known and documented in the DVB-S2 standard.

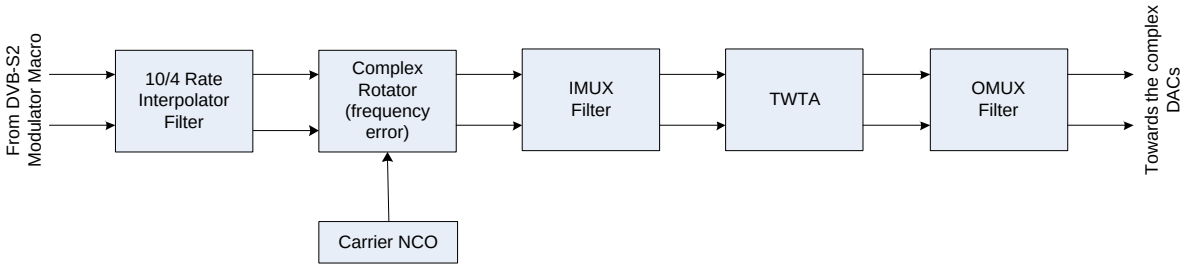

Fig. 3

- The Channel Emulator Macro occupies on the FPGA of the ST SDR, i.e. a STRATIX IV EP4SGX230KF40C3N device, the following Table 4 HW resources.

	Register	Logic	DSP Block	Memory
36MHz Transponder Channel Emulator	3.0%	2.0%	2.0%	2%
Other	1.0%	1.0%	1.0%	1.0%
Free	96.0%	97.0%	97.0%	97.0%
Total	171.000	171.000	1.288	14.625.729

Table 4

- The post layout Timing Analysis of the DVB-S2 Channel Emulator Macro (see Table 5), for the same STRATIX IV ALTERA FPGA shows that the Macro can achieve 30Mbaud (being the Symbol Frequency interpolation section could run as post layout up to 304MHz that at 10 samples per symbol could represent a 30Mbaud Channel Emulator).

Clock Domain	Target Clock Frequency for 27.5Mbaud	Post Layout Clock Frequency	Processing Blocks driven
clk_dac	275MHz	304Mz	The complex sampling rate must be 10 times the max baud rate fixed for HW toggling rate limitations to 27.5Mbaud
service_clk	100MHz	309MHz	Macro service clock for communication and control logic

Table 5

- The Modulator Macro has been tested by ST customer as ACM Modulator in a real 2 way link with Generic Stream Encapsulation Traffic Generator and a DVB-RCS return link. Assuming a given SNIR profile (caused by atmospheric fading during ACM Test) the DVB-S2 Modulator Macro controlled by the SNIR estimation returned on the DVB-RCS channel showed the frame by frame ACM switching capability reported in Fig. 4 while the companion Space Technology Demodulator Macro was maintaining the QeF performances all test session long.

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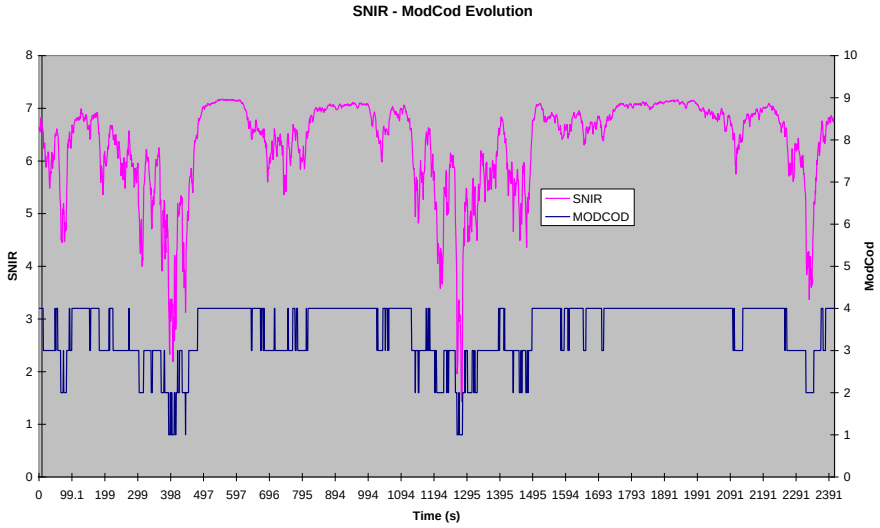

MODCOD	Code
1/4 QPSK	0
1/2 QPSK	1
2/3 QPSK	2
4/5 QPSK	3
3/5 8PSK	4
2/3 8PSK	5
3/4 8PSK	6
2/3 16APSK	7
3/4 16APSK	8
4/5 16APSK	9
5/6 16APSK	10

Fig. 4

- The DVB-S2 Modulator Macro is available either as source VHDL RTL code, as well as structural FPGA configuration file Macro for the FPGAs that can fit its module resources.
- Ultimately note that the DVB-S2 Modulator Macro could fit with the companion DVB-S2 Demodulator Macro in the single 16 cm by 10 cm Software defined radio Board reported on the left side of Fig. 2 (always produced by Space Technology) together with the Channel Emulator so to allow the following Fig. 5 test configuration

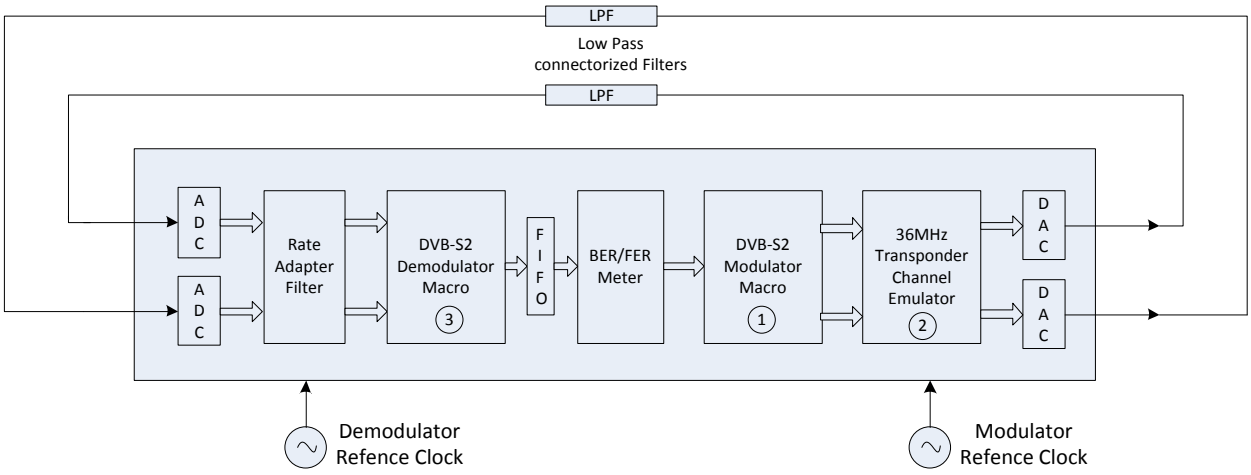

Fig. 5

- The full (Modulator, Demodulator and Channel Emulator) Macro Demonstrator of Fig. 5 occupies on the FPGA of the ST SDR, i.e. a STRATIX IV EP4SGX230KF40C3N device, the following Table 6 HW resources.

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	Register	Logic	DSP Block	Memory
Complete Demonstrator of Fig. 5	70%	53%	42.0%	65%
Other	15.0%	15.0%	10.0%	10.0%
Free	15.0%	32.0%	48.0%	25.0%
Total	171.000	171.000	1.288	14.625.729

Table 6

- The complete forward link of the DVB-S2 could be implemented only when all the Macros of Block 1 and 2 (described in Data Sheet) and the companion Block 3 Macro are purchased. In such a case the Rate Adapter Filter and the FER Meter are provided in the bundle. The Rate Adapter is necessary only when a synchronous test is performed since the Modulator Macro works Base Band at 4 samples per symbol while the Demodulator Macro works Base Band (see companion DVB-S2 Demodulator Data Sheet) at 3 samples per symbol. For a realistic asynchronous test such rate adapter will be bypassed.
- Additionally note that when the Channel Emulator is in the loop the max baud rate will be 27.5Mbaud. Eliminating the Channel Emulator as in Fig. 6 both the DVB-S2 Modulator and Demodulator can be demonstrated at 50Mbaud.

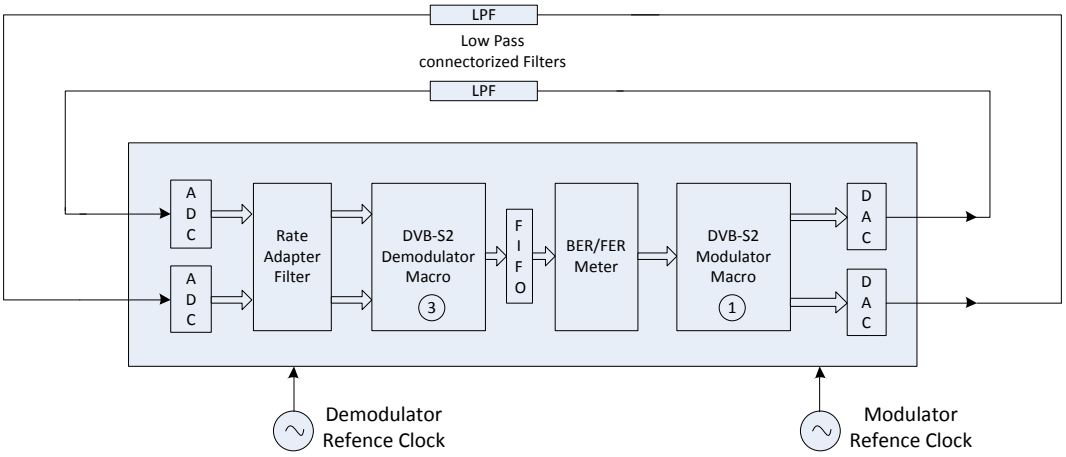

Fig. 6

Note that being an open core DVB-S2 Demodulator, differently from Commercial DVB-S2 Receiver (closed core) when there is a Frame error all the payload bits of the BBFrame affected by a CRC error are discarded while the Space Technology BER Meter does not. Therefore a finer characterization of the Quasi Error Free performance in terms of BER, even if more time consuming is possible.

- The post layout Timing Analysis of the full DVB-S2 Macro Demonstrator configuration of Fig. 5 (see Table 7), based on the the same STRATIX IV ALTERA FPGA provided by the P3U Board shows that the complete Macro could be demonstrated in a single FPGA device up to 27.5Mbaud when the Channel Emulator is included in the Demo Test Bench. When the Channel Emulator between the Modulator and Demodulator is removed as in the Test Configuration of Fig. 6 the full

DVB-S2 macro could run up to 50Mbaud in a single FPGA device based on CMOS 40 nm technology.

Clock Domain	Target Clock Frequency without channel for 50Mbaud	Target Clock Frequency with channel for 27.5Mbaud	Post Layout Clock Frequency	Processing Blocks driven
clk_adc	150MHz	82.5Mz	318Mz	Complex ADC interface BB Filtering (rate adapter and decimator of Fig. 2)
clk_dem1	125MHz	68.75MHz	222MHz	Timing Recovery at greater than 2 samples per symbol (2.5 for 50Mbaud) other blocks see Fig. 3 below
clk_dem2	65MHz	35.75MHz	157MHz	All the blocks at 1 sample per symbol after the Cable Slope Equalizer (Fig. 3)
clk_soft_dem	200MHz	110MHz	202MHz	Soft Demodulator clock
clk_ldpc_dec	150MHz	82.5MHz	206MHz	LDPC Decoder core clock
clk_bch_dec	200MHz	110MHz	241MHz	BCH Decoder core clock
clk_dac	200MHz	275Mz	283Mz	Complex DAC interface BB Filtering four samples per complex symbol without the Channel Emulator @50Mbaud/ The complex sampling rate must be 10 times the max baud rate fixed for HW toggling rate limitations to 27.5Mbaud
clk_byte	60MHz	33MHz	222MHz	This clock is aimed for formatting up to FECFRAME Boarder
service_clk	100MHz	100MHz	112MHz	Macro service clock for communication and control logic

Table 7

- Furthermore, if needed, the Space Technology Design Team is willing to deal any feasible customization of the DVB-S2 Modulator Macro aimed at reducing the FPGA Module count and the power consumption for a lower baud rate application and smaller FPGA devices and/or for fitting the Macro in different FPGA devices other than the one reported in this Data Sheet.
- Finally when the Macro is ported on a different FPGAs, other than the one assembled in the Software Defined Radio Board produced by Space Technology, and is purchased as structural Macro we pre-verify the Macro on one of the available COTS evaluation Board of the FPGA capable of fitting the complexity of the DVB-S2 Modulator and Demodulator macro design. To bypass the fact that typically is not quite simple to find on any target FPGA device a board as compact and furnished with dual wideband ADC and DACs as the Space Technology Board of Fig. 2 we could replace, if the Target FPGA is equipped with High Speed Serial Links (HSSL or equivalent name of SERDES i.e. Serializer Deserialized), the complete Analog DAC and ADC Base Band demonstrator front end as reported in Fig. 7. In this case

the Rate Adapter Filter connecting the HSSL is mandatory to adapt the 4 samples per symbol of the DVB-S2 Modulator output to the 3 samples per symbol necessary at the input of the Demodulator Macro.

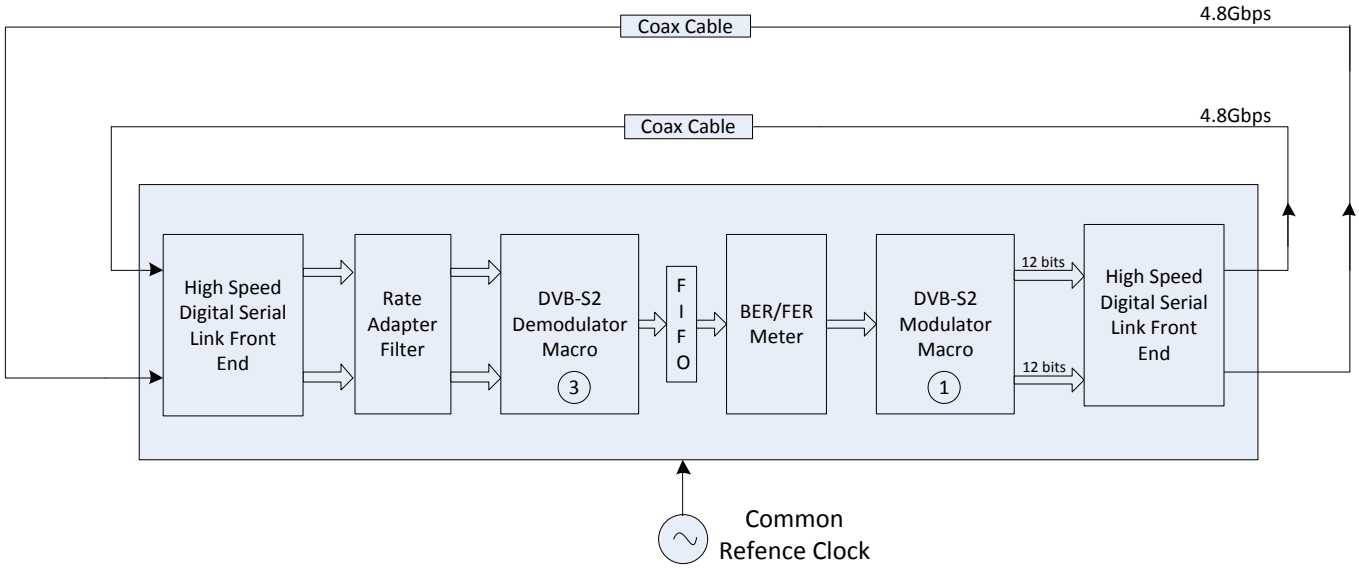

Fig. 7

Finally note that using the Space Technology P3U Board of Fig. 2, the Test configuration of Fig. 7 is possible with only two of the 8 HSSLs available in the SDR Board (each tested at 6Gbps of net through put). In this case the ADC and DAC conversion losses, although very modest, will be completely removed. Sometimes find a COTS Board capable to withstand the test configuration of Fig. 7 might be much easier and cheaper than finding for the same target FPGA device a single Board capable of implementing the test configuration of Fig. 6.

In any case for any scenario configuration different from the one portrayed in this Data Sheet consult our support for a technical and commercial solution tailored on your needs.

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